REMARKS

The above Amendments and these Remarks are in reply to the Office Action mailed September 29, 2005.

Currently, claims 1-57 are pending. Claims 1-10, 12-25, 29-31, 33, 36, 40, 41, 43, 46, 48-52, 54 and 55 are amended. Regarding claims 1 and 14, see, e.g., Fig. 15. Regarding claims 25 and 36, see the specification, page 4, lines 16-20. No new matter is entered.

Claims 1 and 14 are amended to clarify that each particular non-volatile storage element is categorized into one of three different groups based on a detected behavior, and a different programming condition is used for each of the different groups. Other minor clarifying amendments are also made.

Applicants respectfully request reconsideration of the pending claims.

Applicants acknowledge the indication that claims 46-57 are allowed, and that claims 6-11, 18, 19, 28, 33, 39, 42 and 43 include allowable subject matter.

Claims 1-5, 12-17, 20-27, 29-32, 34-38, 40, 41, 44 and 45 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,924,663 to Matsui et al. Applicants respectfully traverse the rejection.

Claim 1 sets forth a method for programming non-volatile memory in which particular non-volatile storage elements in a set of non-volatile storage elements are categorized into three or more groups, each particular non-volatile storage element is categorized into one of the groups based on its detected behavior, and a different programming condition is used for each of the different groups.

In contrast, Matsui et al. are concerned with a programmable logic device (PLD) which uses ferroelectric configuration memories. The configuration memories are divided into groups so that they can be loaded concurrently with multiple configuration data streams (abstract). For example, Fig. 1 indicates that the PLD may include three functional blocks, namely programmable logic blocks 1, programmable interconnections 2 and programmable I/O blocks 3. The non-volatile ferroelectric memories 4, 5 and 6 store the information (configuration data) that defines how to configure the functional blocks 1, 2 and 3, respectively (col. 5, line 55-col. 6, line

1). In particular, each of the ferroelectric memories 4, 5 and 6 stores a plurality of configuration data sets, one of which is selected by a data selector 7, 8 or 9, respectively (col. 6, lines 16-20).

In page 3 of the Office Action, the Examiner asserts that the features of claim 1 are provided by Fig. 1, and col. 1, line 35-col. 2, line 25 of Matsui et al. However, Applicants respectfully submit that there is no basis for this conclusion. The cited passage only refers to the fact that programmable logic devices can be of three types. The first type includes devices having programmable logic blocks, interconnections, I/O blocks, and volatile configuration memories. The second type includes non-volatile configuration memories. The third type uses programmable logic arrays and non-volatile configuration memories. The remainder of the cited passage gives examples of the programmable logic devices and discusses their shortcomings in terms of a limitation in the number of logic gates per unit chip area (col. 2, lines 18-23). To address these shortcomings, Matsui et al. note that the devices can store multiple sets of configuration data.

However, this passage provides no disclosure or suggestion of Applicants' claimed invention. For example, there is no mention of categorizing particular non-volatile storage elements in a set of non-volatile storage elements into three or more different groups based on detected behaviors of the particular non-volatile storage elements. For example, while the device 10 of Fig. 1 of Matsui et al. provides separate ferroelectric memories 4, 5 and 6, and each memory stores different configuration data, there is no categorizing of particular non-volatile storage elements based on their detected behaviors. Instead, the configuration memories 4, 5 and 6 are physically fixed in their respective groups at the time of manufacture, regardless of any detected behavior. The Examiner is respectfully requested to indicate where the reference discloses or suggests categorizing of particular non-volatile storage elements based on their detected behaviors, or to withdraw the rejection. Even if, arguendo, each configuration data set or each ferroelectric memory in Fig. 1 of Matsui et al. is considered to be a set of non-volatile storage elements as set forth in claim 1, there is simply no disclosure or suggestion that each particular non-volatile storage element is categorized into one of the three or more different groups based on a detected behavior as claimed.

Finally, claim 1 sets forth programming particular non-volatile storage elements using a different programming condition for each of the different groups, that is, the different groups into

which the particular non-volatile storage elements were categorized. The Examiner should not confuse the programming of a particular non-volatile storage element, as set forth in claim 1, with the configuring of a programmable logic device using configuration data which was programmed into a configuration memory, as provided by Matsui et al.

Applicants' approach allows the programming process to be adapted based on the behavior of the storage elements (specification, page 4, lines 9-11, page 16, lines 9-18). In particular, the storage elements are programmed using a different programming condition for each group. This approach can result in various benefits including a reduced threshold voltage distribution (page 10, lines 14-18).

Accordingly, it is respectfully submitted that claim 1 and the associated claim 14 are clearly patentable over Matsui et al.

Regarding the related dependent claims, these are also clearly patentable over Matsui et al. For example, claims 2, 3 and 15 set forth that different bit line voltages are applied for the different groups, that is, the different groups into which the particular non-volatile storage elements were categorized. The Examiner cites col. 1, line 22-col. 2, line 9 as providing this feature. However, Applicants have considered this cited passage as well as the reference as a whole and simply do not see any disclosure or suggestion of the feature of applying different bit line voltages to different groups into which particular non-volatile storage elements were categorized. Similarly, claims 4 and 16 set forth that relative programming speeds of particular non-volatile storage elements are determined, and each of the different groups into which the particular non-volatile storage elements were categorized include particular non-volatile storage elements with similar relative programming speeds. Matsui et al. only mention that ferroelectric memory is particularly suitable for programmable logic device applications because of its advantage in operation speed (col. 2, lines 1-3). However, this hardly amounts to a disclosure or suggestion of determining relative programming speeds of particular non-volatile storage elements for use in categorizing as claimed. Likewise, claims 5 and 17 set forth that programmability of particular non-volatile storage elements is determined, and each of the different groups into which the particular non-volatile storage elements were categorized include particular non-volatile storage elements with similar programmability. Again, Matsui et al.

provide no disclosure or suggestion of the claimed feature. The Examiner is respectfully requested to provide clarification or withdraw the rejection.

Claim 25 and the associated claim 36 relate to applying initial programming to non-volatile storage elements until at least one non-volatile storage element reaches a target threshold value, and subsequently, adjusting programming of at least a subset of non-volatile storage elements that have not reached the target threshold value based on behavior of the non-volatile storage elements that have not reached the target threshold value. For example, the adjusting can be based on a characterizing of the non-volatile storage elements that have not reached the target threshold value (claim 26 and 37). Or, the adjusting can include raising bit line voltages (claims 28 and 39), increasing a rate of increase of a common program voltage (claims 29 and 40), determining programmability (claims 32 and 42), and charging and discharging bit lines (claim 33 and 43).

It does not appear that the Examiner has specifically addressed claims 25 and 36. Regarding the citation of Fig. 8, col. 6, lines 8-62 and col. 8, lines 12-21 of Matsui et al. at page 4 of the Office Action, Fig. 8 shows the state of control signals in different operation modes of a ferroelectric memory (col. 4, lines 64 and 64). Col. 6, lines 8-62, and lines 50-62 in particular, refer to a source voltage monitor circuit that detects when there is a sufficiently high voltage for the ferroelectric memories to accept control signals, or to begin data recall operations, when the system power is turned on. Col. 8, lines 12-21 refer to reducing the time of loading memory and starting up the device. However, none of these passages provides any disclosure or suggestion of the claimed features. The invention set forth in claims 25 and 36 adjusts the programming of a subset of non-volatile storage elements that have not reached a target threshold value, after at least one non-volatile storage element reaches a target threshold value using an initial programming. For example, an adjustment can be made in the programming of the non-volatile storage elements which are relatively slow to program. Furthermore, the adjustment is made based on a behavior of these non-volatile storage elements.

Based on the above, withdrawal of the rejection under Matsui et al. and reconsideration of the claims is respectfully requested.

The Examiner's prompt attention to this matter is greatly appreciated. Should further questions remain, the Examiner is invited to contact the undersigned attorney by telephone.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 501826 for any matter in connection with this response, including any fee for extension of time, which may be required.

Respectfully submitted,

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